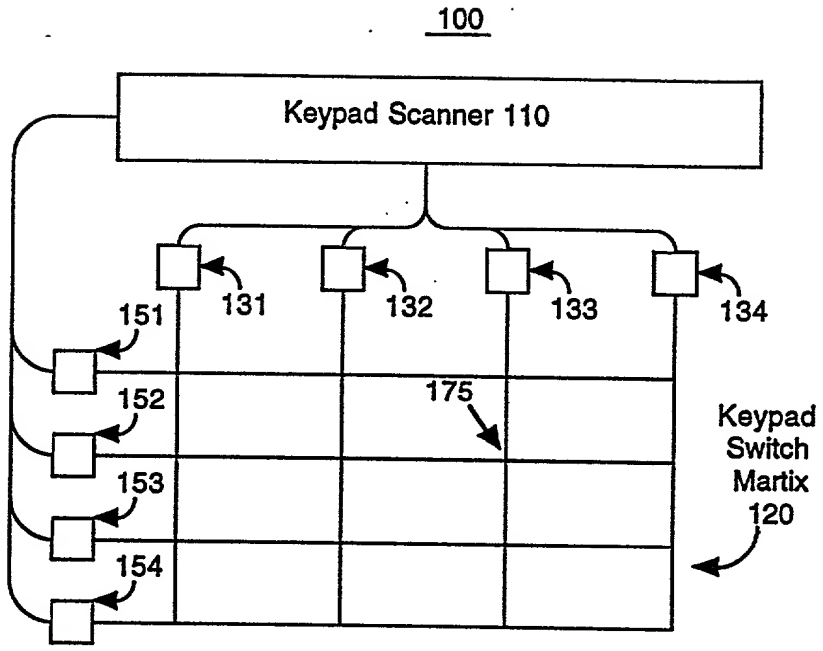
100
Keypad Scanner 110
131
132
133
134
151
152
153
154
175
Keypad
Switch
Martix
120

FIG 1 A

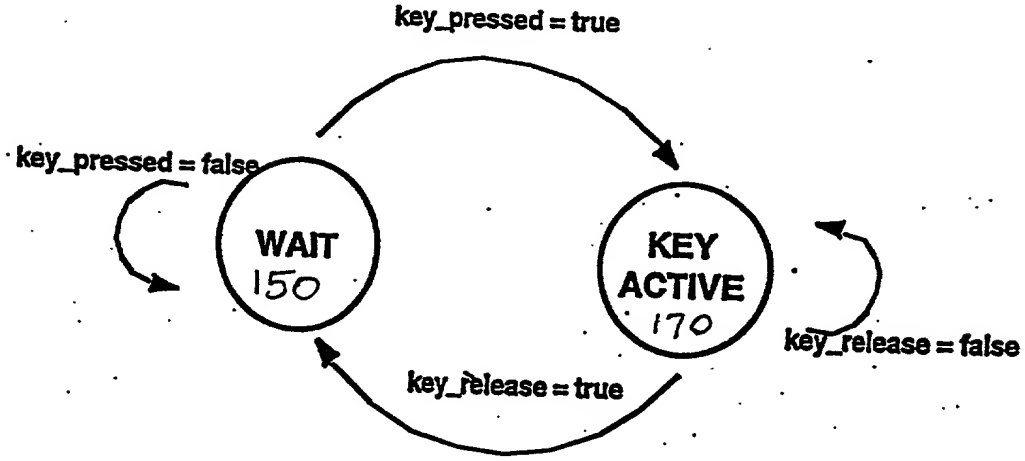
key_pressed = true
key_pressed = false
WAIT
150
KEY
ACTIVE
170
key_release = false
key_release = true

FIG 1B

200

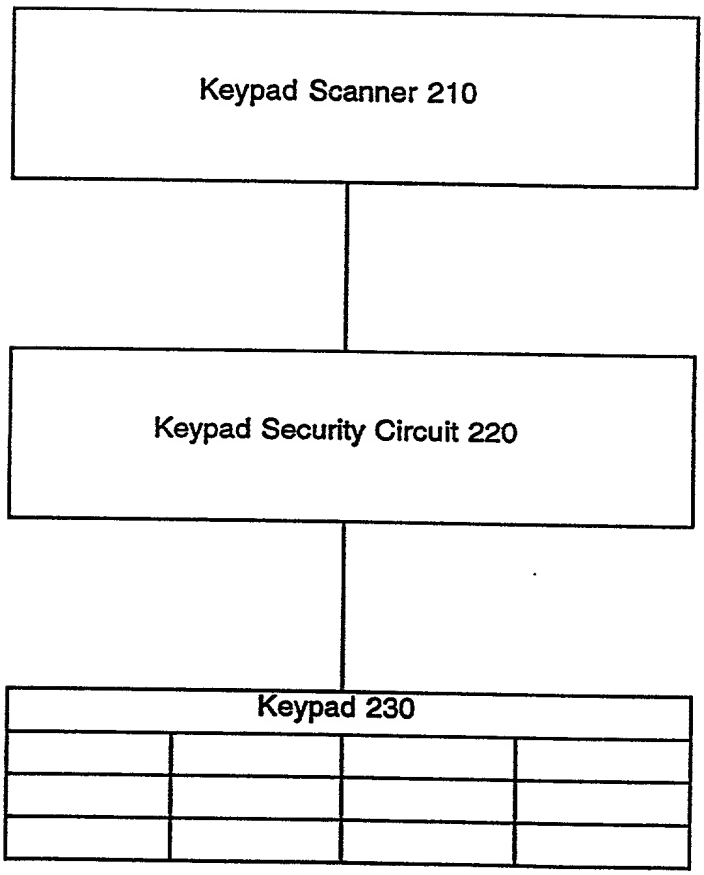

FIG 2

300

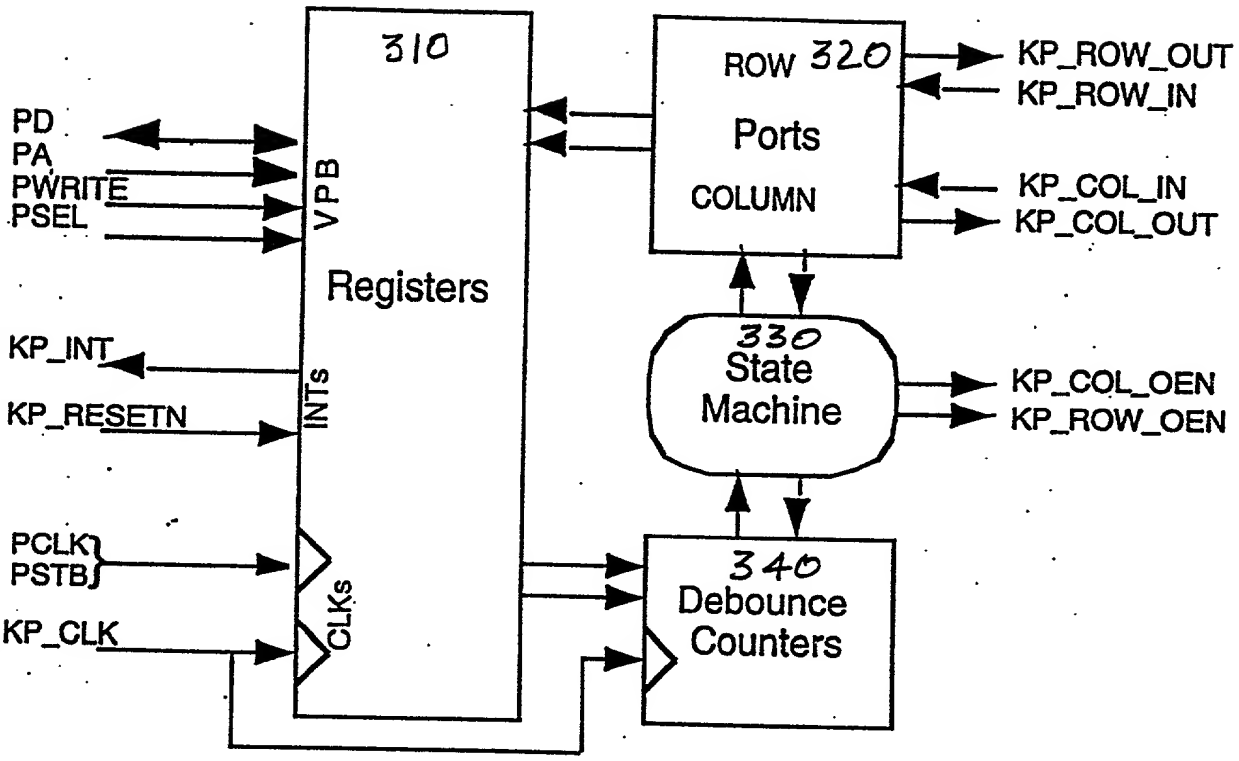
310
Registers
VPB
INTs
CLKs
PD
PA
PWRITE
PSEL
KP_INT
KP_RESETN
PCLK
PSTB
KP_CLK
ROW 320
Ports
COLUMN
KP_ROW_OUT
KP_ROW_IN
KP_COL_IN
KP_COL_OUT
330
State Machine
KP_COL_OEN
KP_ROW_OEN
340
Debounce Counters

FIG 3

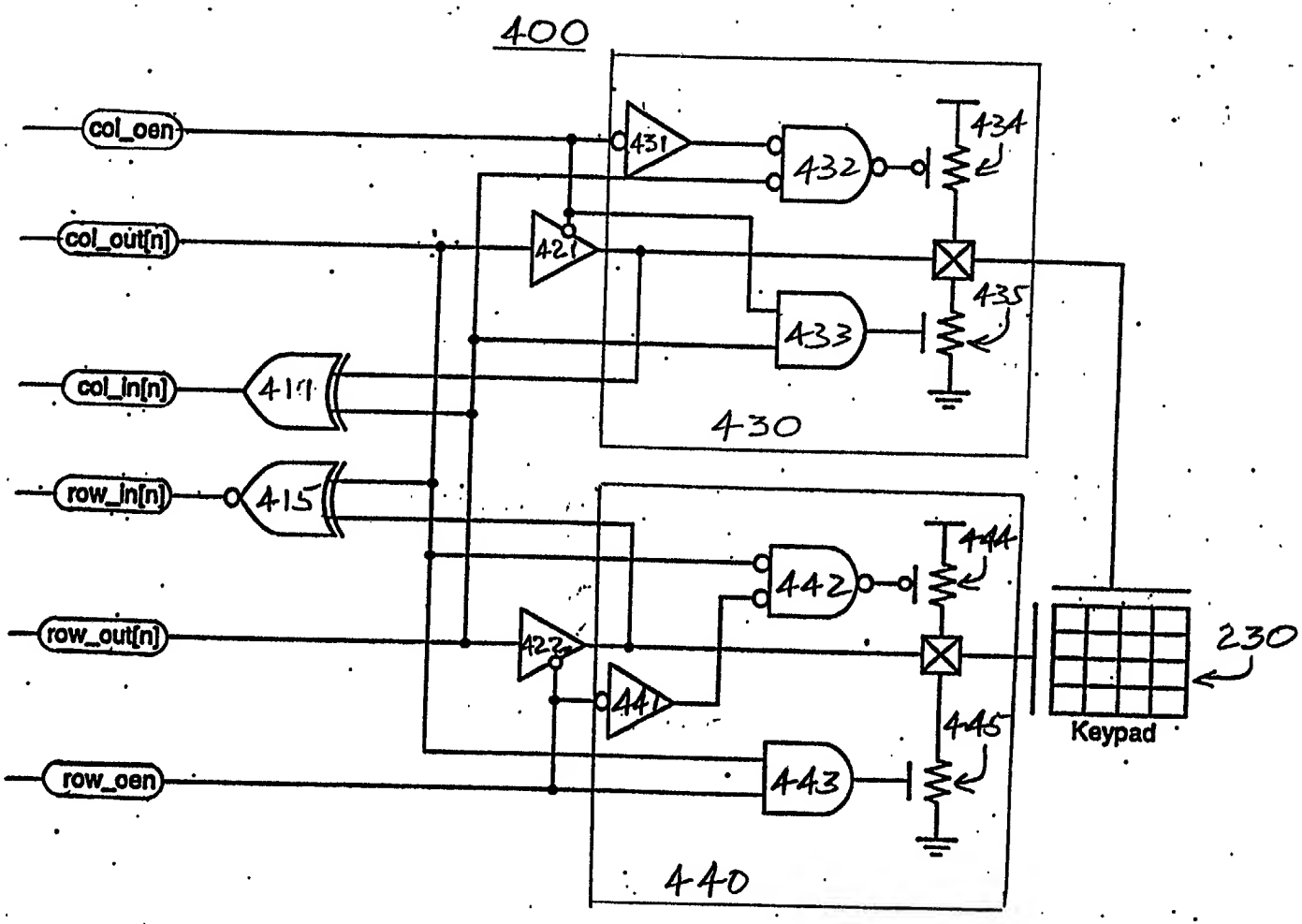
400
col_oen
col_out[n]
col_in[n]
row_in[n]
row_out[n]
row_oen
431
432
434
421
433
435
411
430
415
444
442
422
441
445
443
440
230
Keypad

FIG 4

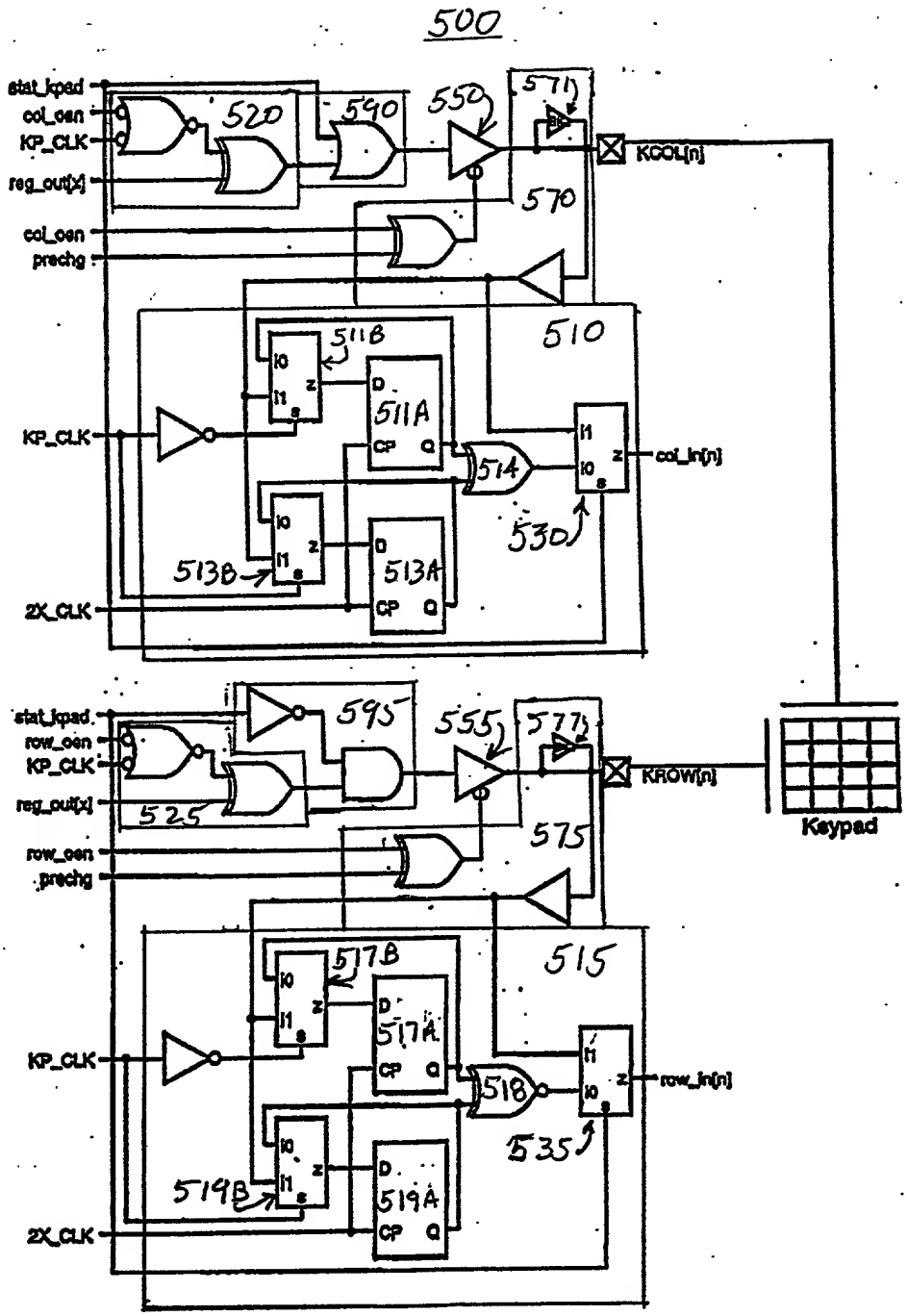
500
stat_kpad
col_oen
KP_CLK
reg_out[x]
520
540
550
571
KCOL[n]
570
col_oen
prechg
510
511B
511A
KP_CLK
514
col_in[n]
530
513B
513A
2X_CLK
stat_kpad
row_oen
KP_CLK
reg_out[x]
595
555
577
KROW[n]
525
575
Keypad
row_oen
prechg
515
517B
517A
KP_CLK
518
row_in[n]
535
519B
519A
2X_CLK

FIG 5

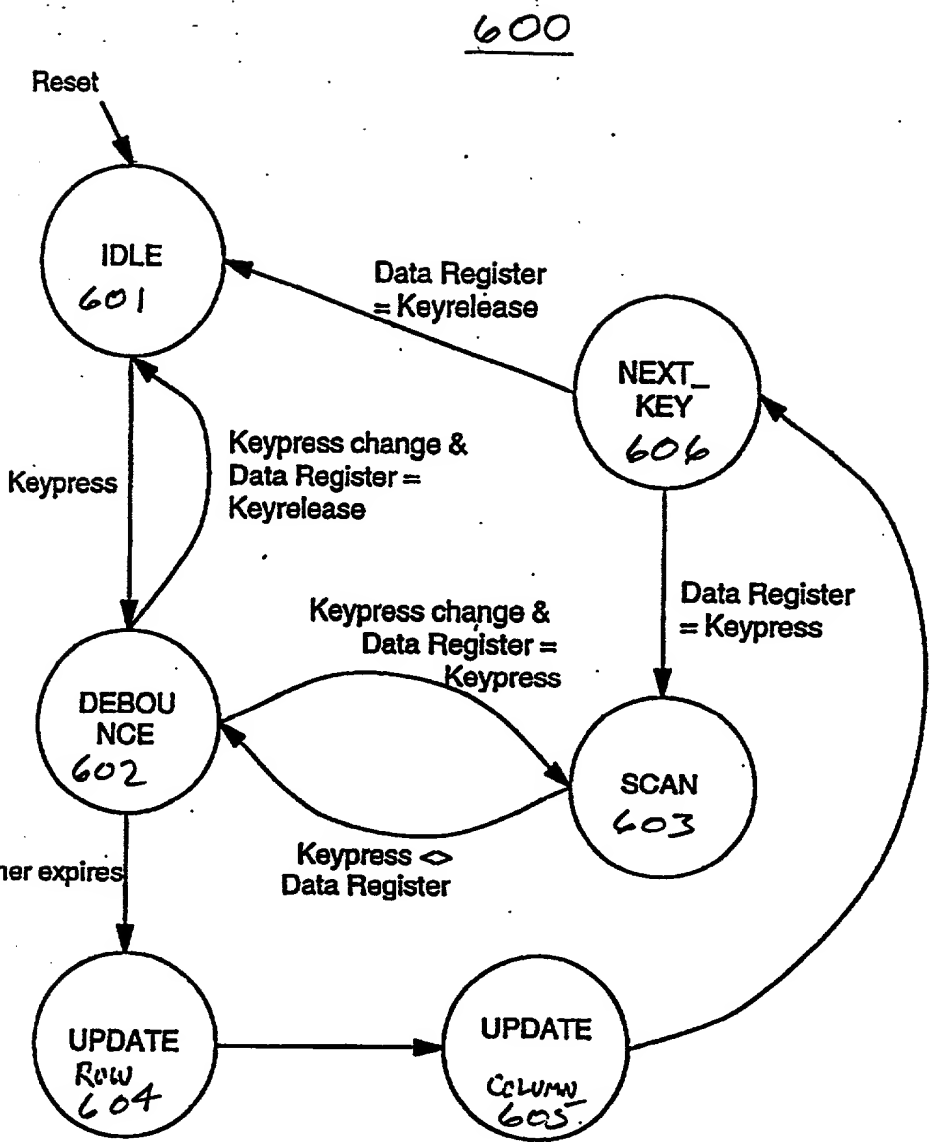
600
Reset
IDLE
601
Data Register
= Keyrelease
NEXT_
KEY
606
Keypress
Keypress change &
Data Register =
Keyrelease
Data Register
= Keypress
Keypress change &
Data Register =
Keypress
DEBOU
NCE
602
SCAN
603
Keypress <>
Data Register
Timer expires
UPDATE
Row
604
UPDATE
Column
605

FIG 6A

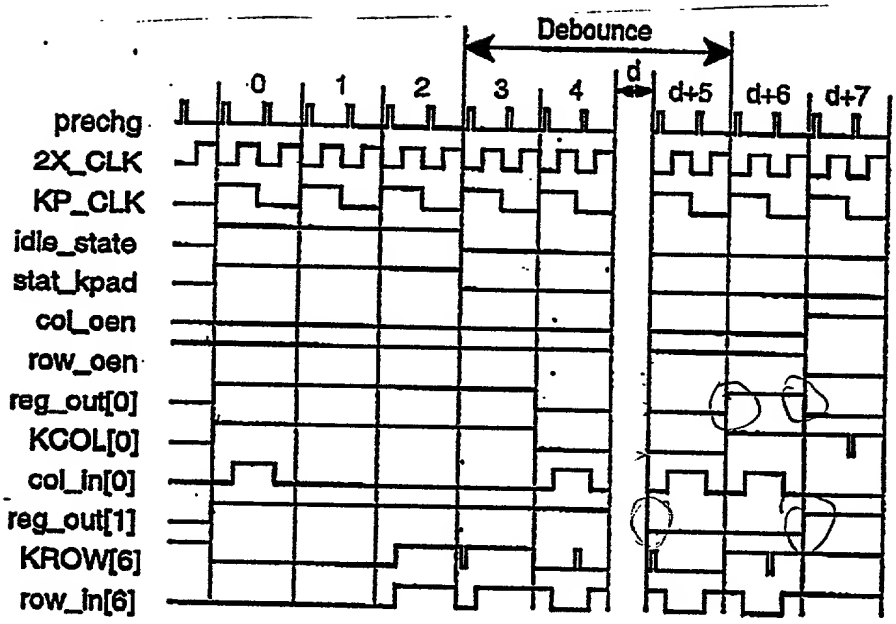
Debounce
0
1
2
3
4
d
d+5
d+6
d+7
prechg
2X_CLK
KP_CLK
idle_state
stat_kpad
col_oen
row_oen
reg_out[0]
KCOL[0]
col_in[0]
reg_out[1]
KROW[6]
row_in[6]

FIG 6B

VPB_base+keyconfig+0h (04000000h+000xx000h+10h=040xx010h thru 040xx04Ch)

	D15	D14	D13	D12	D11	D10	D9	D8
	R							
POR	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	PAD_DRV							
POR	0	0	0	0	0	0	0	0

Bit	Name	Function
15:8	R	Reserved. These bits always return zero.
7:0	PAD_DRV	Pad drive data. Data driven out on either ROW[7:0] or COL[7:0]. The output (row or column) is driven with the data and the input (column or row) is pulled up or down, in the opposite direction of the data. 0 = drive the output low, pull up the input 1 = drive the output high, pull down the input

VPB_base+keyconfig+0h (04000000h+000xx000h+50h=040xx050h)

	D15	D14	D13	D12	D11	D10	D9	D8
	LFSR_DATA[15:8]							
POR	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	LFSR_DATA[7:0]							
POR	0	0	0	0	0	0	0	1

Bit	Name	Function
7:0	LFSR_DATA	LFSR load data. This write only register provides parallel load data to the DATAIN connections of the LFSR.

FIG 7

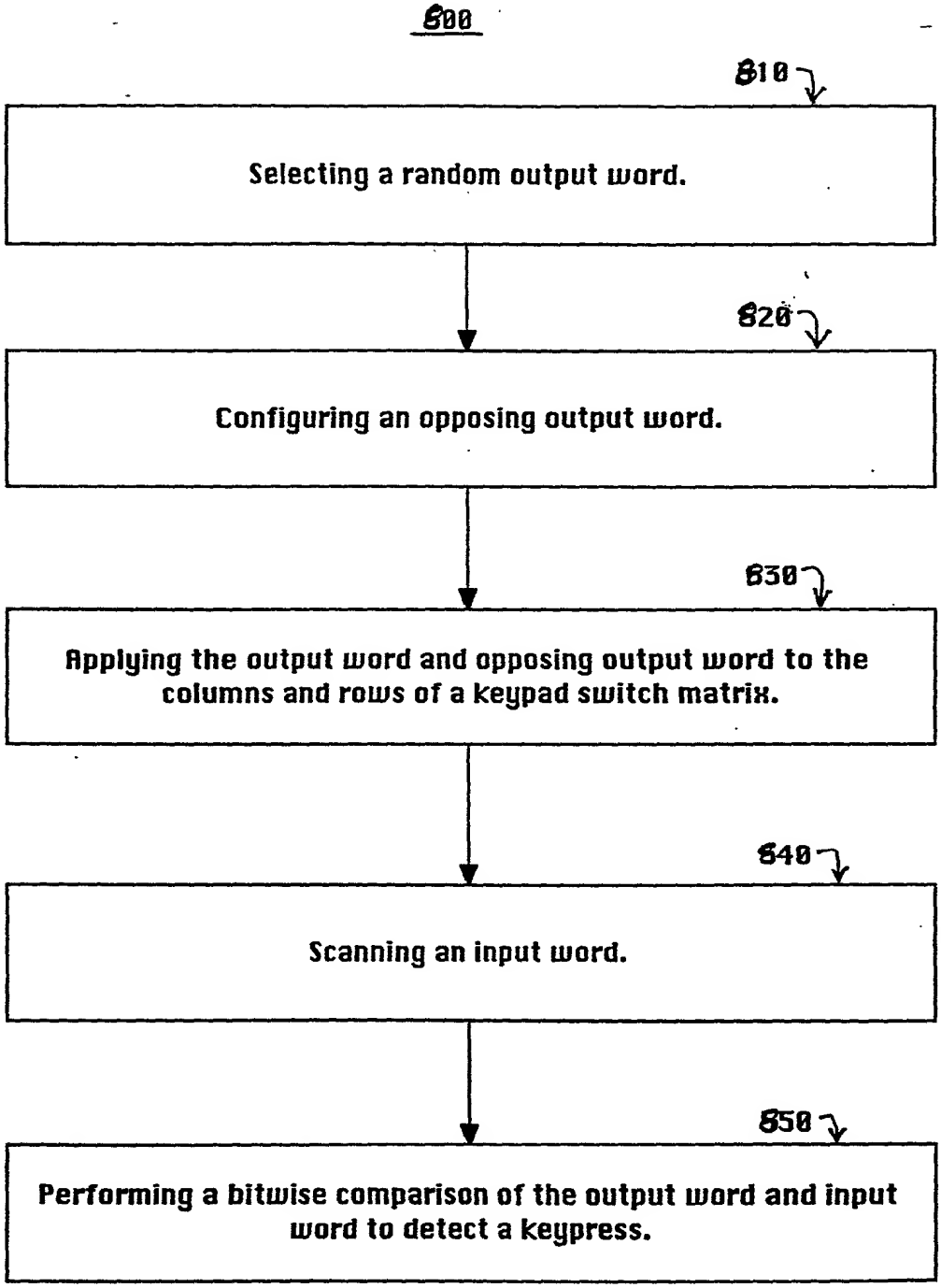
800
810
Selecting a random output word.
820
Configuring an opposing output word.
830
Applying the output word and opposing output word to the columns and rows of a keypad switch matrix.
840
Scanning an input word.
850
Performing a bitwise comparison of the output word and input word to detect a keypress.

FIG 8